A 94 GHZ MONOLITHIC DOWNCONVERTER IN A MESFET TECHNOLOGY

J.-M. Dieudonné*, R. Rittmeyer*, B. Adelseck*, A. Colquhoun+

* Telefunken SystemTechnik, D-7900 Ulm, FRG
+ Telefunken Electronic, D-7100 Heilbronn, FRG
+ now with the Daimler Benz Research Center, D-7900-Ulm, FRG

Abstract

A fully monolithic GaAs 94 GHz downconverter consisting of a single balanced diode mixer and a two-stage IF amplifier has been fabricated in a MESFET technology on a single chip. A conversion gain of 14.5 dB combined with a double side band noise figure of 6.5 dB has been achieved at 94 GHz. This is the first developed single chip MMIC 94 GHz downconverter in a MESFET technology.

Introduction

The development of GaAs millimeter-wave MMICs is a key factor for the low cost, high volume production and size reduction of millimeter-wave systems. A technology, which allows the integration of Schottky diodes and MESFETs on the same chip, has been developed and has been successfully used for the realisation of 60 GHz mixers, IF amplifiers and receiver chips [1] [2]. This technology allows the integration of MESFET oscillators, varactor multipliers, diode mixers and IF low noise amplifiers. This paper presents results on a fully integrated 94 GHz downconverter which consists of a single balanced diode mixer and a two-stage IF amplifier. A typical conversion gain of 14.5 dB combined with 6.5 dB double side band noise figure at a 93 GHz LO frequency and a 1 GHz IF frequency has been achieved. This is the first reported MMIC 94 GHz receiver realized in a MESFET technology on a single chip. The reported results have been obtained in a one pass design and show the validity of the design method, using technology based Schottky diode equivalent circuit and harmonic balanced analysis, and also prove the maturity of the technology for millimeter-wave applications.

Technology

The technology for the monolithic integration of both planar Schottky diodes and GaAs MESFETs has been described in a previous paper [2]. Figure 1 shows the schematic cross-section of a planar Schottky diode. The technology includes a n^+ buried layer, which is formed by selective implantation, to reduce the diode series resistance. An active n layer and a further n^+ layer are deposited by MOCVD. The active layer is used for both the MESFET devices and the Schottky diodes. Isolation of the individual devices is carried out by selective Boron implantation into the n^+/n epitaxial layers. Electron-Beam lithography was used to expose the fingers of the Schottky diodes and the gates of the MESFETs. Both devices are recessed simultaneously. A minimum structure size of 0.3 μm is obtained. All devices are passivated by a plasma-deposited Si_3N_4 layer, which is also used for the insulator in the MIM overlay capacitors. The technology includes both airbridges and via holes. Ft values up to 2.3 THz for the Schottky diodes and Fmax values of 90 GHz for MESFETs have been achieved.

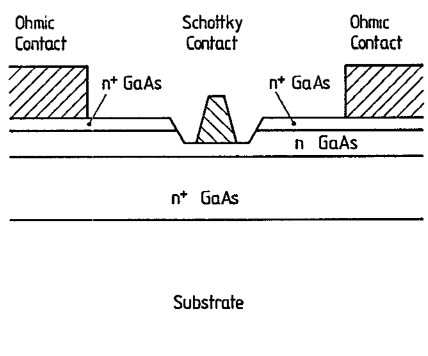

Fig.1: Schematic cross-section of a planar Schottky diode.

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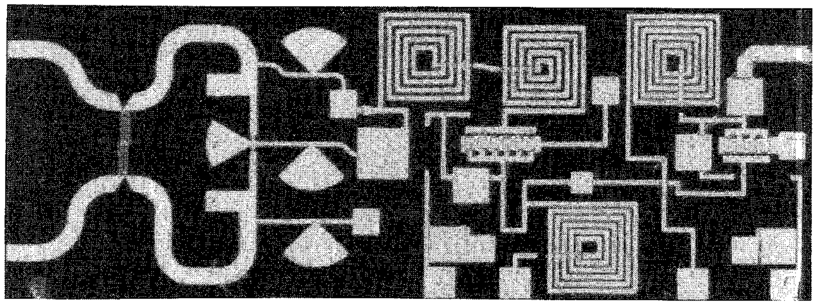
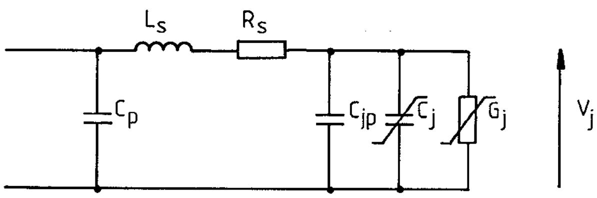


Fig.2: Photo of the 94 GHz MMIC downconverter.

Circuit design

A photo of the realized downconverter is shown in figure 2. A balanced mixer configuration, comprising a pair of Schottky diodes, a Lange coupler and matching networks, has been used in the design of the downconverter. A precise model of the Schottky diode has been developed according to the structure of figure 1. Taking into account the technological parameters, each element of the diode equivalent circuit, shown in figure 3, has been described by an analytical equation [3]. The voltage dependent junction capacitance C_j and conductance G_j of the Schottky contact are described by the classical relations given in the figure. The ideality factor n and the built-in potential V_{bi} are depending on the technology. These two parameters have been measured using the I-V



$$C_j = \frac{C_{jo}}{\left(1 - \frac{V_j}{V_{bi}}\right)^{\gamma}}$$

$$G_j = \frac{q I_o}{nkT} \exp\left(\frac{q V_j}{nkT}\right)$$

Fig.3: Equivalent circuit of the Schottky diode.

characteristic of different diodes. Typical values of 0.83 V for the built-in potential and 1.22 for the ideality factor have been obtained. The internal parasitic junction capacitance C_{jp} is caused by the fringing effects, which are not negligible for a small Schottky contact area. The parasitic resistance R_S is composed of the ohmic contact resistance, the resistance between Schottky and ohmic contact, the resistance under the junction and the resistance of the finger metalization. Due to the planar configuration, the parasitic inductance L_S is assumed to be zero. The external parasitic capacitance C_p represents the coupling capacitance between ohmic and Schottky contact metalizations.

The diode model is implemented in a large signal analysis program based on the harmonic balanced technique [4] [5]. The diode is analyzed as a single ended mixer to determine the optimum matching impedances of the RF and image frequencies for good conversion loss and noise figure. It is assumed that the RF excitation is negligibly small compared to the LO, so the large signal analysis is performed under LO excitation only. The Fourier series coefficients of the junction capacitance and conductance of the diode are calculated for the mixing frequencies and the conversion matrix is derived. At this step of the analysis the appropriate diode geometry is chosen. In order to reduce the LO power consumption a one finger diode with an area of $0.3 \times 5\ \mu m^2$ was used. After the large signal analysis, the complete single balanced mixer can be designed and the IF output impedance is calculated to be matched to the IF amplifier. RF and LO ground and IF filter have been realized by using radial stubs.

The in house software to calculate the microstrip discontinuities and the radial stubs has been improved for the millimeter-wave frequency range.

A Lange coupler is used to reduce the chip dimensions. The coupler design is based on published theory [6]. A separated fabricated Lange coupler shows a transmission loss of about 4.5 dB at 94 GHz. The mixer circuit is designed for self bias operation.

Because the diode mixer exhibits conversion loss, it increases the contribution of the IF amplifier noise to the noise figure of the complete receiver. In order to obtain optimum receiver noise performance, it is important to minimize the noise figure of the IF amplifier. The desired frequency range of the IF amplifier is 0.5 - 2 GHz. It is a two stage low noise amplifier employing MESFET devices with a gate length of 1 μm. The transistor in the first stage has 12 fingers and a total gate width of 840 μm to achieve a low device noise figure. The device in the second stage has 8 fingers with a total gate width of 560 μm. The equivalent circuits of the 2 transistors were derived from S-Parameter measurements. Unconditional stability was obtained by using resistive feedback for the two stages. The on chip bias circuits consist of a 2000 Ω series resistance and a shunt capacitance for each gate and a series inductance for each drain.

A network consisting of a DC blocking capacitance, a shunt capacitance and a series inductance transformed the output impedance of the mixer into the required minimum noise reflection coefficient of the amplifier.

Experimental results

Mixer, amplifier and downconverter chips have been fabricated on a 0.1 mm thick GaAs substrate. Figure 2 shows the realized downconverter. The chip size is 4 x 1.5 mm^2. DC and IF returns of the mixer are realized with via holes.

Figure 4 shows the measurement results of the separately fabricated mixer. A double side band noise figure of 4 dB combined with 6 dB conversion loss was achieved at a LO frequency of 93 GHz and an IF frequency of 1 GHz. These results represent state of the art performances for a monolithic single balanced diode mixer in the W-band. The conversion loss is improved of 1 dB compared to the first 94 GHz mixer realized with a branch line coupler [7].

The gain and the noise figure of the separately fabricated IF amplifier are shown in figure 5. At a frequency of 1 GHz the noise figure is 1.8 dB combined with 22 dB gain.

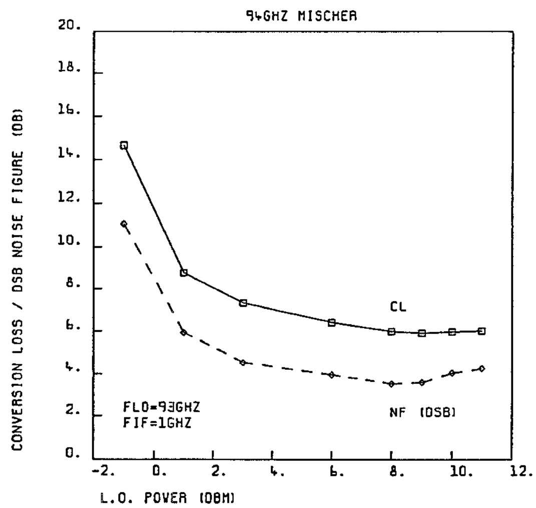


Fig.4: Conversion loss and double side band noise figure of the mixer versus LO power.

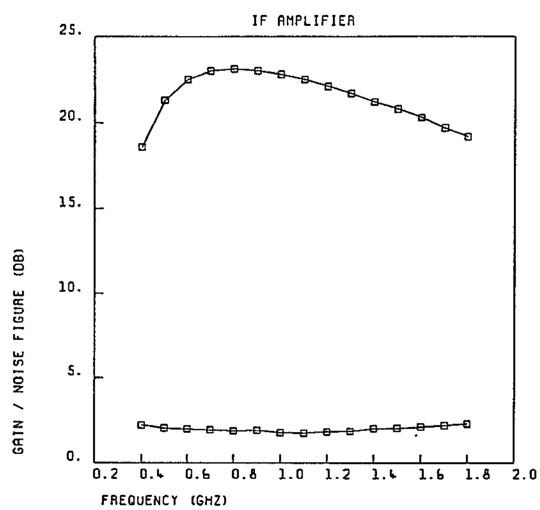


Fig.5: Noise figure and gain of the IF amplifier.

Figures 6 and 7 show the measured conversion gain and double side band noise figure of the downconverter as a function of the IF frequency and the LO power respectively. The mixer operates in self bias mode. The downconverter exhibits a conversion gain of 14.5 dB with 6.5 dB double side band noise figure at 93 GHz LO frequency and 1 GHz IF frequency. The noise figure is below 6.5 dB and the gain is greater than 13.5 dB for a 0.5 GHz-1.5 GHz IF frequency range. The downconverter can be driven by low LO power levels.

Conclusion

A GaAs monolithic integrated 94 GHz downconverter consisting of a single balanced diode mixer and a two-stage IF amplifier has been fabricated in a MESFET technology on a single chip. A conversion gain of 14.5 dB and a DSB noise figure of 6.5 dB were measured at 94 GHz. The whole downconverter is a one pass design. This is the first developed single chip MMIC 94 GHz downconverter in a MESFET technology. The downconverter results show the maturity of the technology for millimeter-wave applications.

Acknowledgements

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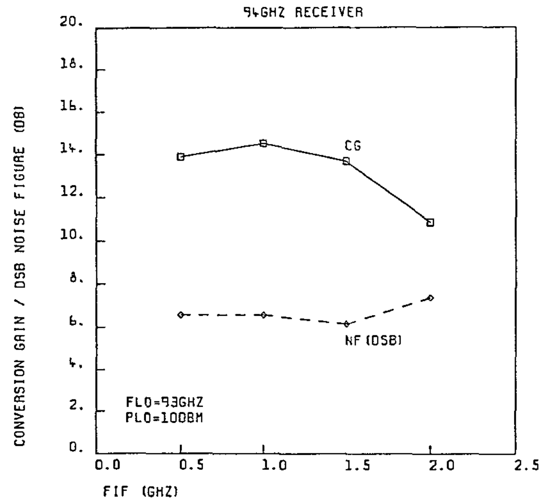

Fig.6: Conversion gain and DSB noise figure of the MMIC downconverter versus IF frequency.

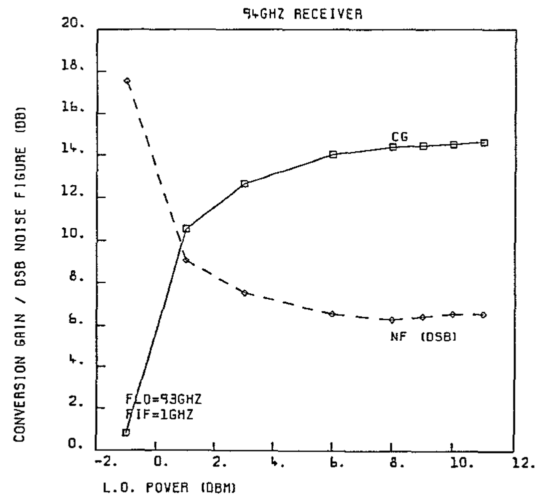

Fig.7: Conversion gain and DSB noise figure of the MMIC downconverter versus LO power.